potential; and

a third diffusion layer of the second conduction type fabricated at a bottom of the second diffusion layer, the third diffusion layer being connected to the second diffusion layer,

the first diffusion layer being circularly enclosed with the second and third diffusion layers.

Please add the following new claims 21-27:

21. (New) An input/output protection device for a semiconductor integrated circuit, said protection device comprising:

a substrate having a first conduction type;

a first region having a second conduction type opposite said first conduction type, said first region connected to an input/output terminal;

a second region enclosing said first region, said second region having said second conduction type, said first region and said second region being electrically separated;

a third region formed adjacent said second region, said third region having said second conduction type; and

a fourth region surrounded by said substrate and said first, second, and third regions, said fourth region having said second conduction type.

22. (New) The protection device of claim 21, where an impurity concentration of said fourth region decreases in a direction away from said first region.

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23. (New) The protection device of claim 21, wherein said second region is connected to a first constant electrical potential.

24. (New) The protection device of claim 21, further comprising a MOS gate structure for providing electrical separation between said first and second regions, said MOS gate structure including a gate electrode connected to a second constant electrical potential.

25. (New) The protection device of claim 23, further comprising a fifth region electrically isolated from said third region, said fifth region having said first conduction type, said fifth region connected to said first constant electrical potential.

26. (New) An integrated circuit having an input/output protection device of claim 21.

27. (New) The protection device of claim 1, wherein a protection of said internal circuit occurs by an avalanche breakdown in which said first diffusion layer connected to said input/output terminal serves as a collector and said second and third diffusion layers serve as an emitter for a lateral bipolar transistor.

REMARKS

Attached hereto is a marked up version of the changes made in the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"